

Attorney Docket No. 42P8534C

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)	
)	
Jin Yang)	Examiner: Unassigned
)	
Application No.: Unassigned)	Art Unit: ***
)	
Filed: Herewith)	
)	
For: SYMBOLIC MODEL CHECKING)	
WITH DYNAMIC MODEL)	
PRUNING)	
)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Express Mail No: EV33586078US

Date of Deposit: September 17, 2003

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

- X 37 C.F.R. §1.97(b).
- 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:
- A statement pursuant to 37 C.F.R. §1.97(e) or
- A check for \$180.00 for the fee under 37 C.F.R. § 1.17(p).
- 37 C.F.R. §1.97(d). If so, then enclosed with this Information Disclosure Statement are the following:
- (1) A statement pursuant to 37 C.F.R. §1.97(e); and
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If there are any charges due, please charge them to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: September 17, 2003


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Substitute for Form 1449A/PTO (Modified)	Attorney Docket No.: 42P8534C	Application Number: Unassigned
Sheet 1 of 4	First Named Inventor: Jin Yang	Examiner: Unassigned
	Filing Date: Herewith	Art Unit: Unassigned

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
		5,119,318		Paradies et al.	06/02/1992	
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		6,339,837		Li	01-15-2002	
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		B1				
Examiner Signature					Date Considered	

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Sheet 2 of 4	Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 42P8534C	Application Number: Unassigned
		First Named Inventor: Jin Yang	Examiner: Unassigned
		Filing Date: Herewith	Art Unit: Unassigned

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
		BEREZIN, S. et al, "A Compositional Proof System for the Modal μ -Calculus and CCS," <i>Technical Report CMU-CS-97-105, Carnegie Mellon University, January 15, 1997</i>	
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		BURCH, J. R. et al, "Representing Circuits More Efficiently in Symbolic Model Checking," <i>28th ACM/IEEE Design Automation Conference, Paper 24.3, 1991, pages 403-407</i>	
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		CHAN, W. et al, "Combining Constraint Solving and Symbolic Model Checking for a Class of Systems with Non-linear Constraints," <i>Computer Aided Verification, 9th International Conference, CAV '97 Proceedings (O. Grumberg, Editor), Lecture Notes in Computer Science 1254, pages 316-327, Haifa, Israel, June 1997. Springer-Verlag (Revised in December '98)</i>	
		CHEN, Y. et al, "PBHD: An Efficient Graph Representation for Floating Point Circuit Verification," <i>Technical Report CMU-CS-97-134, Carnegie Mellon University, May 1997</i>	

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		CHEUNG, S. et al, "Checking Safety Properties Using Compositional Reachability Analysis," <i>ACM Transactions on Software Engineering and Methodology</i> , Vol. 8, No. 1, January 1999, pages 49-78	
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		CLARKE, E. et al, "Another Look at LTL Model Checking," <i>Technical Report CMU-CS-94-114, Carnegie Mellon University</i> , February 23, 1994	
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		CLARKE, E. M. et al, "Formal Methods: State of the Art and Future Directions," <i>ACM Computing Surveys</i> , Vol. 28, No. 4, December 1996, pages 626-643	
		CLARKE, E. M. et al, "Model Checking and Abstraction," <i>Proceedings of the 19th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages</i> , February 1992, pages 343-354	
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		JACKSON, D., "Exploiting Symmetry in the Model Checking of Relational Specifications," <i>Technical Report CMU-CS 94-219, Carnegie Mellon University</i> , December 1994	

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Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
		JAIN, A. et al, "Verifying Nondeterministic Implementations of Determinist Systems," <i>Lecture Notes in Computer Science, Formal Methods in Computer Aided-Design</i> , pp. 109-125, November 1996	
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		KERN, C. et al, "Formal Verification In Hardware Design: A Survey," <i>ACM Transactions on Design Automation of Electronic Systems</i> , Vol. 4, No. 2, April 1999, pages 123-193	
		KURSHAN, R. et al, "Verifying Hardware in its Software Context," <i>Proceedings of the 19th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages</i> , February 1992, pages 742-749	
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		Zhang Z., "An Approach to Hierarchy Model Checking via Evaluating CTL Hierarchically," <i>IEEE Proceedings of the Fourth Asian Test Symposium</i> , Nov. 24, 1995, pages 45-49.	

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